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Novel high performance DC reactor type fault current limiter

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ABSTRACT

This paper presents a novel structure for DC reactor type fault current limiter (DRFCL), which can suppress the fault current in distribution networks. The proposed DRFCL is composed of a DC reactor, a bridge rectifier, and anti-paralleled IGBTs power electronic (PE) switch. The DC reactor contains main and supplementary windings. The main winding has a high inductance and acts as a DC reactor. The supplementary winding is used as a control means for fast FCL operation. The fast response allows the cost, weight and volume of the DC reactor to be reduced. The proposed DRFCL reduces the overvoltages on the devices and it has lower number of components, therefore, it can be economic. Analytical solutions, to describe the performance of the proposed DRFCL are presented and the proposed model is simulated via MATLAB software. Finally, a one-phase prototype structure is built and experimental results are studied to show the capability of the proposed DRFCL.

1. Introduction

It is well known that distribution network's power quality, reliability and protection are important for utility and customers. Limiting the fault current amplitude reduces the stress on devices, improves the PCC voltage level, decreases the voltage drop on elements, etc. When a fault occurs, the result is a fault current flow, PCC and load voltage drop and other severe insulation problems. Such transient phenomenon will shorten the lifetime of distribution network equipments, and may damage circuit breakers or electromagnetic switches. Moreover, the fault current may cause an abnormal operation of transformers and sensitive loads, and results in lower power quality [1–4]. Various approaches have been proposed for limiting the fault current and preventing the insulation failure problems, such as employing single-use fuse [5–7], series current limiting reactor [8], series transformer [9], and also superconductive limiter [10–12]. These solutions may cause other problems such as series resonance, need for an additional control circuit, and more power losses during the steady state operation mode, and complexity of control strategy. Hence, solid state fault current limiters (SSFCLs) have been commonly studied and suggested for distribution networks to provide a better equipment protection. Besides the SSFCLs, DC reactor type FCLs have been suggested with different control approaches [13]. For example, single-phase DC reactor-type FCL has been studied in [14]. But this FCL needs a DC bias power supply and the inductance of the FCL winding is low as compared with the suggested DRFCL winding. The size of the FCL winding and DC bias power supply of [14] increases the FCL cost and also weakens the FCL response to the first peak of the fault current. Other improved topologies have been studied in [15–18] but in these FCLs, the mentioned problems have not been solved. A single-phase FCL employing IGBT bidirectional switch has been reported in [19]. The switch has been realized using a stack of IGBT and anti-parallel diode. Also, varistors have been used in parallel with switches as a voltage clamping element. The main disadvantages of this FCL are high conduction loss of the IGBT switch in normal operation mode and the switch overvoltage which is higher than the line peak voltage. Also, the varistor is required to dissipate a rather significant power. A transformer inrush current limiter based on DC reactor has been studied in [20]. The bridge-type FCLs with reduced number of controlled devices for inrush current limitation has been given in [21]. In order to reduce the magnitude of inrush current, a bidirectional impedance-type inrush current limiter (BIT-ICL) is proposed in [22]. Application of new control strategy to improve the fault ride through capability of doubly fed induction generator (DFIG) during the symmetrical and asymmetrical grid faults is studied in [23]. The smart fault current mitigation solutions and voltage sag analysis are given in [24]. Fault level consideration is an important factor for the interconnection of distributed generation (DG) to the electrical network [25]. In this paper, the calculation of the resulting fault level in medium and low voltage distribution networks with DG is discussed. Using FCL as a constraint for properly dispatch of active power in the power

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system is given in [26]. Employing a new family of zero-energy sag correctors to realize protection against voltage sag has been presented in [27,28] and the design guidelines for such sag correctors for the new dynamic voltage restorer (DVR) system have been provided. The DVR, as a means of series compensation for mitigating the effect of voltage sags, has been established as a preferred approach for improving power quality [29] and also, the combination of FCL and DVR for decreasing the requested power rating and time response of abnormal variations at DVRs have been proposed. In [30], the DVR and resistive type high temperature superconducting fault current limiter (HTS-FCL) have been designed and implemented as a series grid interface topologies for enhancing the fault ride-through (FRT) performance of doubly fed induction generator (DFIG)-based wind turbines (WTs).

In order to overcome the shortcomings of the DC reactor response problem and decrease the FCL cost, this paper proposes a DC reactor type FCL to increase the FCL response to the first peak of the fault current while the inductance of the DC reactor is high as compared with other conventional DRFCLs [14–18]. The fast response allows the inductance, cost, weight, and volume of the DC reactor to be accordingly reduced. This paper has been organized as follows: in Section 2, the proposed distribution network configuration including DRFCL and its operation principles has been presented. The analysis of the proposed DRFCL has been developed in Section 3, and Section 4 discusses the simulation results and Section 5 includes experimental results of the built prototype. Finally, last section gives the conclusion and highlighted merits of the proposed DRFCL.

2. Distribution network configuration and operation principles

2.1. Distribution network and DRFCL configurations

The single-line diagram of a two feeders power system including DRFCL is shown in Fig. 1. It is assumed that the feeder F1 supplies a sensitive load and the feeder F2 delivers power to other loads. After fault occurrence in F2, the rapidly increased fault current causes a voltage sag at the PCC. For controlling the fault current and maintaining the PCC voltage at an acceptable range, a novel DRFCL is proposed, which is composed of a DC reactor with two windings, an anti-paralleled IGBT switch, a single-phase bridge rectifier, a DC voltage source (V_b) for compensation of DRFCL power losses and a simple control circuit.

The suggested FCL employs a DC reactor with two windings that act as a transformer. The main winding has a relatively high inductance and the second one (supplementary winding) has less winding turns. In usual DC reactor based FCL, it can be saturated by the induced DC voltage on the DC reactor during normal operation mode. The saturated DC reactor shows negligible impedance and FCL has negligible effect on the system voltage, current and power quality. However, the size of the DC reactor is a great challenge because high inductance DC reactor has a considerable delay in the instant of the circuit breaker energization. Furthermore, we suggest a novel DC reactor based FCL with high inductance and good current limiting capability. During normal operation mode, the supplementary winding is short-circuited via antiparallel IGBTs. Furthermore, the short-circuited supplementary winding bypasses the main winding and FCL inductance does not cause any delay in the system energization instant. Other DRFCL stray inductances are saturated via induced DC voltage form DRFCL rectifier bridge. Therefore, during normal operation mode, the DRFCL losses are negligible and the stray inductances are saturated and are short-circuited completely. Finally, the DRFCL main and supplementary windings are short-circuited via connected IGBTs but they are not saturated. Therefore, the DRFCL employs a DC reactor with high inductance and fast performance. The saturated inductances include main and supplementary stray inductances.

The first winding of the DC reactor (main winding) is placed between PCC and the electrical load, and its main function is to insert high impedance into the line at the instant of fault occurrence. Moreover, the DC reactor short circuit rate and the fast response of the DRFCL are related to the secondary winding (supplementary winding) operation and can be changed by adjusting its turns ratio. So, it provides best electrical isolation and a fast performance for the DRFCL as well. The main winding of the DC reactor has a high inductance and its core is made of silicon steel, without any air gap, which short-circuits in normal operation mode and reduces the voltage drop across the DRFCL. In normal operation mode, for reducing power losses, the IGBT switches turn-on and after transient removal, the output voltage of the bridge rectifier short-circuits the remains inductances and these switches turn-off automatically.

2.2. Operation principles

To explain the operating principles in normal and fault conditions, the proposed DRFCL can be simplified to the circuit shown in Fig. 2.

According to the DC reactor charging and discharging behavior, its operation modes are described as follows:

Normal operation mode: After closing the CB, the diode pairs D_1–D_2 and D_3–D_4 conduct in positive and negative half cycles respectively. So the output DC current of the bridge charges the DC reactor up to the AC current level. Prior to start-up, the control circuit of the anti-paralleled IGBTs turns the switches on. Therefore, the supplementary winding is short-circuited which bypasses the main winding. Furthermore, the linkage inductance of the DC reactor is short circuited by the high flowing DC current and the DRFCL is invisible during normal operation mode. Then the short-circuited DC reactor turns off IGBTs in next interval. During this period, the DC reactor voltage freewheels and acts as a short circuit presenting low impedance. The DRFCL has direct connection to the voltage source with a negligible voltage drop, and the current of the line flows through the diodes shown in Fig. 2(a).

Fault current limiting mode: This mode can be divided into the following two sub-modes:

(a) Limiting sub-mode: When a downstream short-circuit fault occurs, the rising AC fault current reaches the DC reactor current level and the diodes, which are carrying the fault current, remain in ON state and other two diodes are in OFF state at zero current. When a pair of diodes (D_1 and D_2 or D_3 and D_4) conduct at the instant of fault occurrences, the fault current flows through the DC reactor. In this case, the supplementary winding of the DC reactor is open-circuited because its supply voltage is fed from node n, and voltage of this node is near zero. Therefore, the IGBTs driver circuit is bypassed and these switches are turn-off during the fault, as shown in Fig. 2(b). Due to increase in the DC reactor reactance, the magnitude of the fault current will be limited below the expected value and the CB can take protective action.

(b) Freewheeling sub-mode: After suppressing the fault current, voltage of node n back to the pre-fault value and the supplementary winding is again short circuited via IGBT switches. In this mode, the DC reactor discharges via the diode rectifier rapidly. Then, all diodes (D_1–D_4) turn on simultaneously. In this mode, the DC reactor freewheels and acts as a short circuit. The load has a direct connection to the line, and the current of the line flows through the diodes as shown in Fig. 2(a). Because of the supplementary winding of the DC reactor and IGBT switches operation, the DC reactor is charged

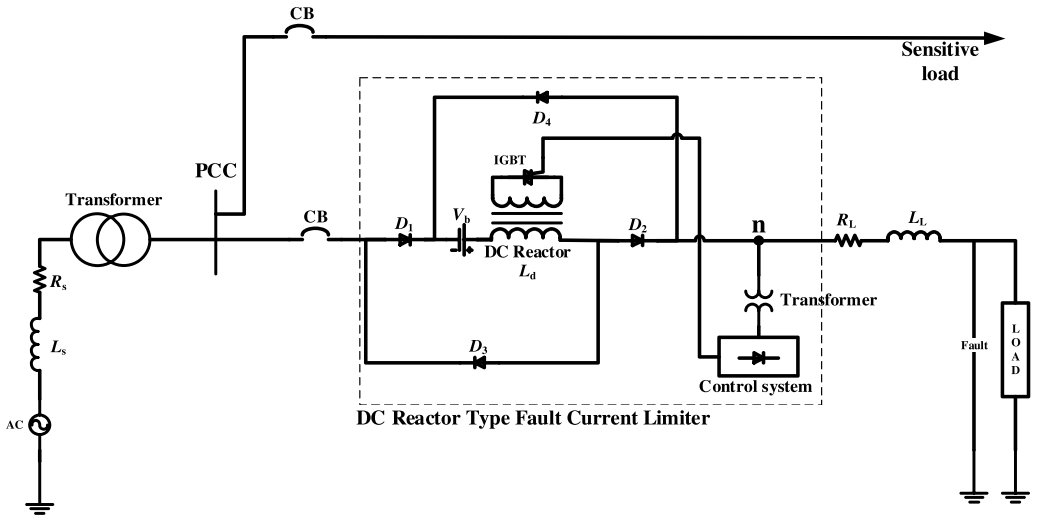

Fig. 1. Single-line diagram of distribution network including the proposed DC reactor type fault current limiter.

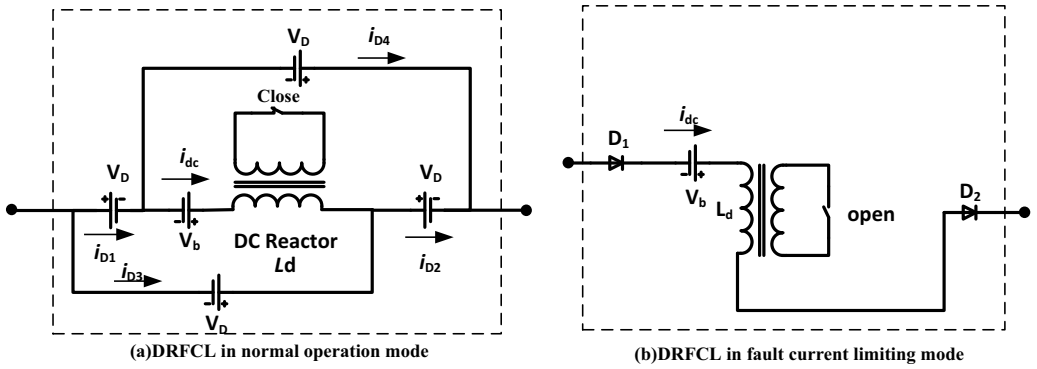

Fig. 2. DRFCL (a) normal operation and (b) fault current limiting modes.

and discharged rapidly every half cycle during the steady-state operation mode, and the line current waveform is not distorted. The supplementary winding with IGBT switches acts as a key component for allowing the DC reactor to be bypassed very fast.

3. Analysis of proposed DRFCL

3.1. Circuit analysis

In order to simplify the circuit analysis, the source impedance is neglected, and the DC reactor is assumed to be an ideal one; thus, the short-circuit impedance of the DC reactor is neglected as well. The line current of the proposed DRFCL may have five operation modes:

Transient mode ($t_0 \le t < t_1$): in this state, the CB is closed and the system experiences the transient state.
Normal mode ($t_1 \le t < t_2$): after transients are decayed, the system is in normal mode and DC reactor is completely bypassed.
Limiting sub-mode ($t_2 \le t < t_3$): at t_2, fault occurs and as a result, the line current is increased. During the fault, DRFCL is active and controls the fault current. The equivalent circuit of this mode is shown in Fig. 3 where $i_{line}(t)$ is the line current and circuit equation can be expressed as follows:

$$R_1 i_L(t) + L_1 \frac{di_L(t)}{dt} = V_m \sin(\omega t + \theta) - 2V_D + V_b \quad (1)$$

where $R_1 = R_{line} + R_d$, R_d and R_{line} are the DC reactor and line resistances, respectively. Also, L_1 is equal to $L_d + L_{line}$, which are the DC reactor and line inductances, respectively, V_D is the rectifier diode voltage drop in forward bias and V_b is DC bias source voltage. It is assumed that the diodes turn on at $t = t_0$, and the initial condition is given as follows:

$$i_L(t_1) = I_1$$

Solving (1), the line current can be calculated as follows:

$$i(t) = I_1 e^{-(R/L)(t-t_2)} + \frac{R_1}{{R_1}^2 + (\omega L_1)^2} V_m \sin(\omega t + \theta) - \frac{\omega L_1}{{R_1}^2 + (\omega L_1)^2} V_m \cos(\omega t + \theta) - \frac{2V_D + V_b}{R_1} \quad (2)$$

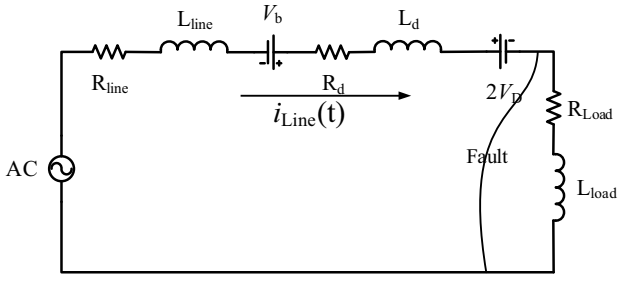

Fig. 3. Proposed network equivalent circuit in fault current limiting mode.

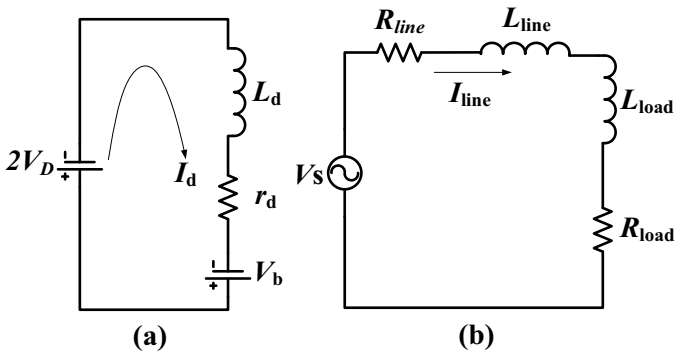

Fig. 4. Equivalent circuit in normal operation mode: (a) DRFCL equivalent circuit and (b) network equivalent circuit.

Freewheeling mode ($t_3 \le t < t_4$): During this mode, the DC reactor discharges and all rectifier diodes are conducting. The current of each diode is given as follows:

$$i_{D_1} = i_{D_2} = \frac{i_{line} + i_d}{2} \tag{3}$$

and

$$i_{D_3} = i_{D_4} = \frac{i_{line} - i_d}{2} \tag{4}$$

where i_d is the DC reactor current and i_{line} is the current of the network line. The equivalent circuit of the normal operation mode is shown in Fig. 4. According to Fig. 4(a), the DC reactor current can be written as follows:

$$L_d \frac{di_d(t)}{dt} + R_d i_d(t) + 2V_D - V_b = 0 \tag{5}$$

The initial value is given as $i_d(t_1) = I_1$, and DC reactor current, $i_d(t)$ can be written as follows:

$$i(t) = I_1 e^{-(R/L)(t-t_1)} - \frac{2V_D + V_b}{R} \tag{6}$$

Steady state ($t_4 \le t < t_5$): In this state, the equations of diode currents, i_{D_1}, i_{D_2}, i_{D_3}, and i_{D_4}, are the same as those in the freewheeling mode of the transient state. Thus, the DC reactor acts as a short circuit during the steady state. As long as the DC reactor current is equal to or higher than the peak value of the line current, D_1 through D_4 will always conduct and thus the DC reactor current will circulate in two loops of the bridge rectifier. As a result, the proposed DRFCL acts as a short circuit in the steady state.

3.2. DC reactor design consideration

For analyzing the system behavior during the fault and studying the effect of the DC reactor on the fault current, the equivalent circuit of the system shown in Fig. 5 is used.

In this model, the source and fault impedances are ignored because its value in comparison with the reactor inductance is very small and can be neglected. In addition, for obtaining the DC reactor current, the value of the electrical source is modeled by its mean value on the DC side. For obtaining the DC reactor current, it is necessary to design the value of the DC reactor inductance. The differential equation of the equivalent circuit shown in Fig. 5 is given as follows:

$$V_{DS} = r_d i_d(t) + L_d \frac{di_d(t)}{dt} \tag{7}$$

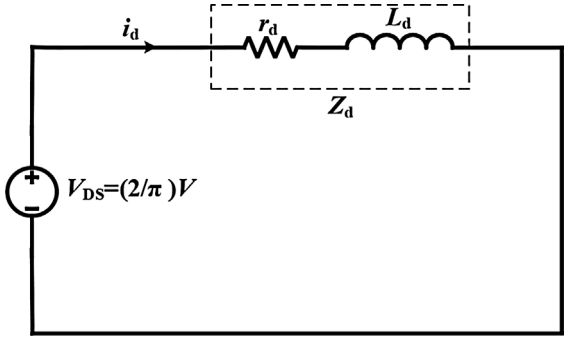

Fig. 5. Equivalent circuit of system during fault.

By solving Eq. (7), the DC reactor current is obtained as given in (8).

$$i_{dc}(t) = \frac{V_{Ds}}{L_d}(t - t_0) + I_{peak} \tag{8}$$

where the initial value of $i_{dc}(t)$ at t_0 is I_{peak} and the effect of the DC reactor losses (r_d) is not considered in (8), because its value in comparison with L_d, is very small. In addition, we have:

$$i_0 = i_d(t = t_0) = I_d \tag{9}$$

where t_0 is the instant of the fault inception and it is assumed that circuit breaker can open the faulty line at t_1. The DC reactor inductance value during normal operation mode should be considered enough, where the DC reactor current flow through the reactor being slightly higher than the normal flow of the AC current through the transmission line. On the other hand, with respect to the nominal values of the power network equipment, the value of the DC reactor inductance should be considered suitable that it can decrease the fault current level to an acceptable level and the circuit breaker successfully opens the faulty line. However, increasing the DC reactor inductance increases the time of its discharge after fault clearance and also increases the system operation delay. By considering t_1 as the necessary time for the circuit breaker to open the faulty line after fault inception and its corresponding current with i_1, we can solve Eq. (7) to obtain Eq. (10) for fault occurrence mode.

$$t_1 - t_0 = \frac{L_d}{r_d} Ln \frac{r_d i_1 - V_{DS}}{r_d i_0 - V_{DS}} \tag{10}$$

In Eq. (10), i_1 is determined via circuit breaker alignment and its capability to open the faulty line. On the other hand, the value of i_1 is determined according to the nominal values of the distribution network equipment. In addition, the time between t_1 and t_0 ($t_1 - t_0$) is the circuit breaker time performance before the current of the power electronic diodes exceeds from i_1. Furthermore, by determining the rectifier bridge output voltage (V_{DS}), t_0 and t_1, it is possible to design the DC reactor inductance and resistance. In addition, the suggested DRFCL can employ high value DC reactor and can control the amplitude of the fault current successfully without generating extra delay and operational cost. Due to the control winding of the DC reactor, it is possible to use the relatively high value DC reactor with fast performance.

3.3. Power losses and stored energy

In order to reduce the DRFCL power dissipation during normal operation mode, the supplementary winding is simultaneously short circuited at the instant of CB energization. The short-circuited winding causes fast DC reactor saturation via the bridge rectifier. So, the steady-state power losses of the proposed DRFCL has the following elements:

DC reactor: Bypassing the supplementary winding in normal operation made causes fast DC reactor saturation and it is assumed that the DC reactor current ripple is negligible, and thus, the steady-state power losses resulting from the DC reactor can be calculated as follows:

$$P_{\text{loss, reactor}} = I_{\text{d}}^2 \times R_{\text{d}} \tag{11}$$

Single-phase bridge rectifier: The steady-state power loss of the bridge rectifier can be expressed by the following equation:

$$P_{\text{loss, rectifier}} = 2V_{\text{D}} \times I_{\text{d}} \tag{12}$$

Two antiparallel IGBT switches: These switches are in on state both in the system normal operation and the system recovery after fault clearance. The voltage drop and related power losses in these switches can be obtained as follows:

$$P_{\text{loss, IGBT}} = V_{\text{sw}} \times I_{\text{supplementary coil}} \tag{13}$$

As a result, combining Eqs. (11)–(13), the total steady-state power losses caused by the DRFCL can be written as follows:

$$P_{\text{loss, total}} = [I_{\text{d}} \times (I_{\text{d}}R_{\text{d}} + 2V_{\text{D}})] + P_{\text{loss, IGBT}} \tag{14}$$

It can be found that reducing the resistance of the DC reactor windings will result in a reduction in the steady-state power losses. Moreover, if it is assumed that the supplementary winding application increases the DRFCL ability in fault current limitation then total power losses during the steady state operation mode are small percentage of the feeder transmit power which can be neglected accordingly. Furthermore, the stored energy in DRFCL in the steady state can be derived as follows:

$$W = \frac{1}{2}L_{\text{d}}(I_{\text{d}}^2) \tag{15}$$

4. Simulation results

In this section, a single line 20 kV distribution network including DRFCL as shown in Fig. 1, is studied. The resistance of the electrical load is 48.4 Ω. The simulation and experimental parameters, which should be used later, are listed in Table 1. It is assumed that the fault current should be limited at around 2 times of the rated line current. The inductance of the DC reactor is 0.5 H, and the DC-bias voltage source is not used. Also, the supplementary winding value is given in this table and it should be short circuited during normal operation mode.

The current value of the DC reactor in normal operation mode is adjusted to be slightly higher than the peak value of the line current as shown in the simulation results. The simulation is accomplished by MATLAB software and the impedance of the voltage source and the line is considered in simulations.

Table 1
Network parameters.

Parameters	Description	Value
V_{s} (experimental)	Source voltage (line-ground) (rms)	220 V
V_{s} (simulation)	Source voltage (line-line) (rms)	20 kV
r_{s}	Source resistance	1 Ω
L_{s}	Source inductance	0.01 H
r_{L}	Line resistance	1 Ω
L_{L}	Line inductance	0.01 H
f	Power system frequency	50 Hz
V_{IGBT}	Voltage drop across IGBT	2 V
V_{D}	Voltage drop across diode	2 V
r_{d}	DC reactor resistance	0.1 Ω
L_{d}	DC reactor inductance	0.5 H
Primary and supplementary windings turn ration	DC reactor windings turn ratio	20:1
R_{load}	Load resistance	48.4 Ω
L_{load}	Load inductance	0.1 H
r_{F}	Fault resistance	0.001 Ω
L_{f}	Fault inductance	0 H
Z_{line}	Line impedance	0.6 Ω

In this section, the normal, fault and current limiting operation modes are simulated. In limiting mode, the effect of supplementary winding on the fault current is studied. In the first mode, the supplementary winding is open circuited and the DRFCL response speed to the fault current is slow, so the fault current amplitude is decreased with considerable delay. In the second mode, the supplementary winding is short circuited during normal operation and is open circuited at the instant of the fault occurrence. The PCC waveform (time domain and RMS values) with and without using the proposed DRFCL is shown in Figs. 6 and 7, respectively.

As shown in Fig. 7, the DRFCL response time to the fault is obviously decreased and the PCC voltage is restored to the specified level faster than the case with open circuited supplementary winding. Due to the DC reactor impedance and the supplementary winding operation, the difference between three simulated PCC voltage drops and also the limited line current is obvious. As shown in these figures, the inductance of the DC reactor plays the main role in fault current limitation and PCC voltage drop recovery. In the case of open circuited supplementary winding, by increasing the DC reactor inductance up to 2 H, the fault current is successfully limited. But the increased value of the inductance increases the response time in the system operation. This problem can be solved via short circuiting the supplementary winding in normal operation mode and also in the case of system recovery after fault clearance. The short-circuited winding bypasses the DC reactor and DC reactor time constant is accordingly decreased. The line current

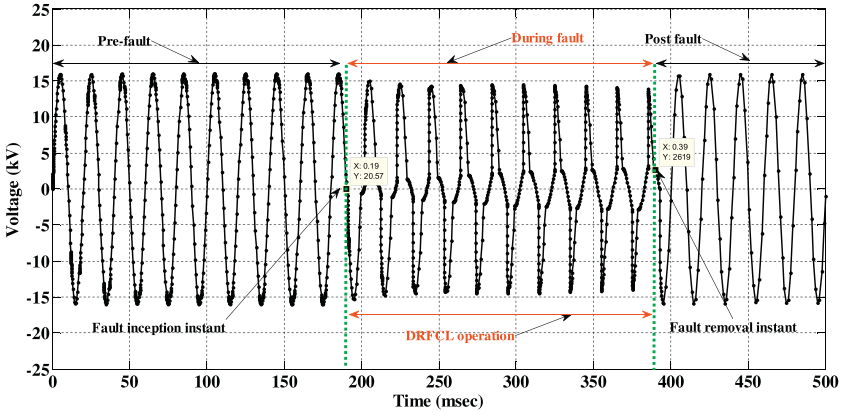

Fig. 6. PCC voltage of proposed network during normal and fault operation modes in time domain.

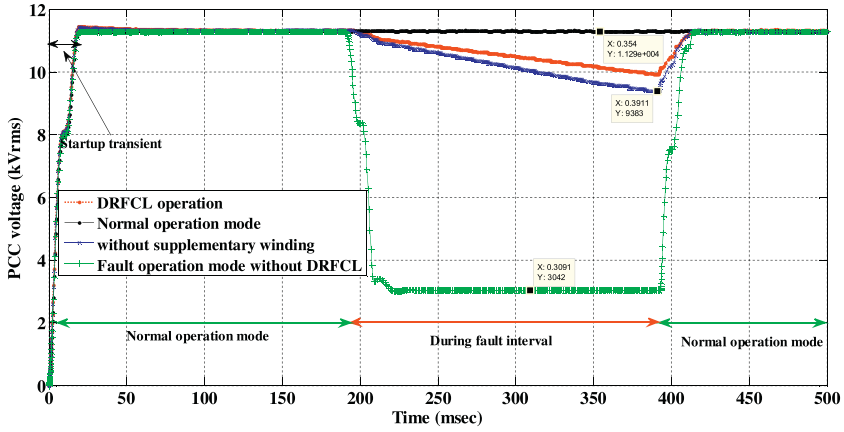

Fig. 7. RMS value of the PCC voltage of proposed network during normal and fault operation modes.

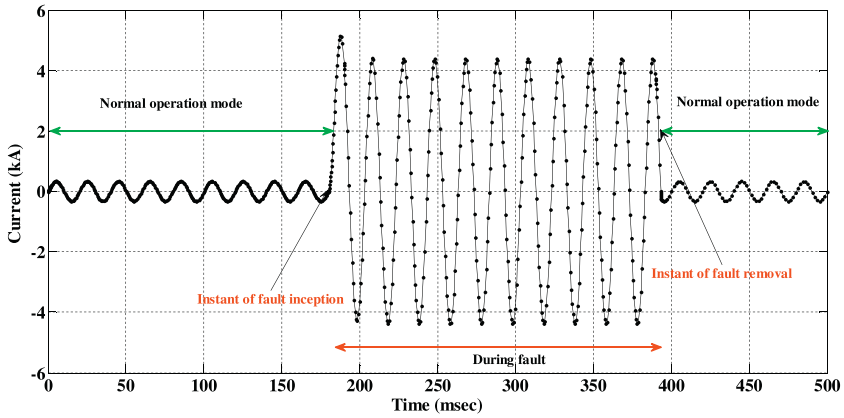

Fig. 8. Line current in pre-fault, during fault and post-fault conditions.

in normal and fault conditions is shown in Fig. 8. Before fault, the line current is sinusoidal and feeds the electrical load.

Before $t = 190$ ms, the system is operating in steady-state mode and after $t = 190$ ms the occurred fault increases the line current up to 5134 A. When the fault occurs and the proposed DRFCL is utilized, it is obvious that the line current, as shown in Fig. 9, can be effectively restrained. In Fig. 9 the effect of the supplementary winding operation on the fault current is shown for two cases. In the first case, it is assumed that the supplementary winding is open, so the DC reactor is connected in series with the line at the instant of CB energization. As shown in this figure in dotted curve, a high value of the DC reactor causes considerable delay in the normal operation mode. In the second case, it is assumed that the supplementary winding is short circuited via the antiparallel IGBTs, therefore, the DC reactor is negligible during normal operation mode, because the short circuited winding bypasses the DC reactor very fast. At fault inception, the power supply of the control circuit is disconnected and the supplementary winding becomes open-circuit. The solid wave shape in Fig. 9 shows the DRFCL operation during normal, fault and post-fault modes. By comparing these two wave shapes, the effectiveness of the supplementary winding application is obvious. The improved structure of the DRFCL can increase the DC reactor response to the fault limitation and system recovery after fault removal.

Moreover, the DC reactor current at the energization instant with and without supplementary winding application for different DC reactor inductances are shown in Fig. 10(a) and (b). In these figures, the five operation modes of the proposed DRFCL, i.e. periods $t_0 \le t < t_1$, $t_1 \le t < t_2$, $t_2 \le t < t_3$, $t_3 \le t < t_4$ and $t_4 \le t < t_5$ can be seen.

The DC reactor value is changed in three steps and the effect of the inductance increase on the fault current is shown. As shown here, the high value of the DC reactor (2 H) reduces the fault current near to the normal current value but the system operation delay is not acceptable. Also, for 0.2 H, the system delay is acceptable, but its impedance cannot decrease the fault current to an acceptable level. Fig. 10(b) shows the same simulation results while the supplementary winding of the DC reactor is short-circuited during normal operation mode and is open-circuited during the fault. As shown here, during normal operation mode, the rector current is DC and DRFCL has no effect on system power quality. After fault occurrence, the supplementary winding is opened and the DRFCL impedance is rapidly increased. In this figure, the effect of the DC reactor can be seen. The increased value of the reactor inductance can limit the fault current better and the problem of operation delay is solved by using the supplementary winding.

5. Experimental results

Prototype of the system is built as shown in Fig. 11, the parameters of which are listed in Table 2. This prototype consists of a bridge rectifier, a DC reactor including two windings and a simple fault detection circuit.

Using a start/stop switch, a single line to ground fault is modeled. The controlling circuit includes a transformer, a rectifier bridge, a RC filter, a resistive voltage divider, hysteresis block and a reference DC voltage as shown in Fig. 12. In the normal operation mode, the control circuit is connected to the node "*n*" shown in Fig. 1. The network measured voltage is applied to the rectifier bridge, then the output DC voltage is filtered by the RC filter and the filtered

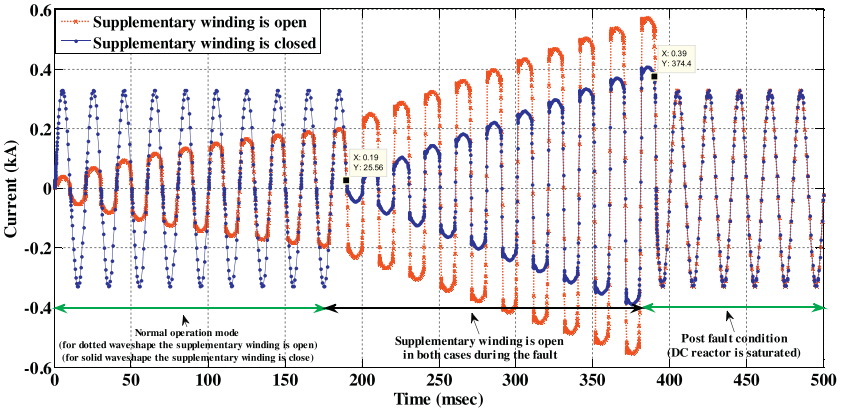

Fig. 9. Line current in normal and faulty operation modes.

Table 2
Experimental setup parameters.

IGBT	Voltage	1200 V
FGH25N120FTDS	Current	25 A
Diode SKN	Voltage	1200 V
26/12	Current	24 A
Distribution	Feeder F1	$j0.314\,\Omega$
feeders data	Feeder F2	$j0.157\,\Omega$
Load data	Sensitive load	$10+j15.7\,\Omega$
	Load of F2	$15+j31.4\,\Omega$
Reactor data	Reactor inductance	0.2 H
	Reactor loss	$0.2\,\Omega$

DC voltage is compared with the reference DC voltage (V_{ref}). If the difference between the generated DC voltage and reference one is near zero, the IGBTs pulses are generated and turn on the switches. At fault inception, the line voltage is decreased to zero and there is no generated DC voltage so the V_{ref} is greater than the DC voltage of the control circuit and IGBTs' pulses are changed and these switches turn off.

Also, the corresponding measured PCC voltage of the prototype system is shown in Fig. 13 and can be compared with Fig. 7. In this figure, the measured PCC voltage is 220 Vrms. During normal operation mode, the voltage is 220 Vrms and DRFCL has negligible effect on network power quality. At fault inception, the PCC voltage is decreased but DRFCL could restore its value to an acceptable level.

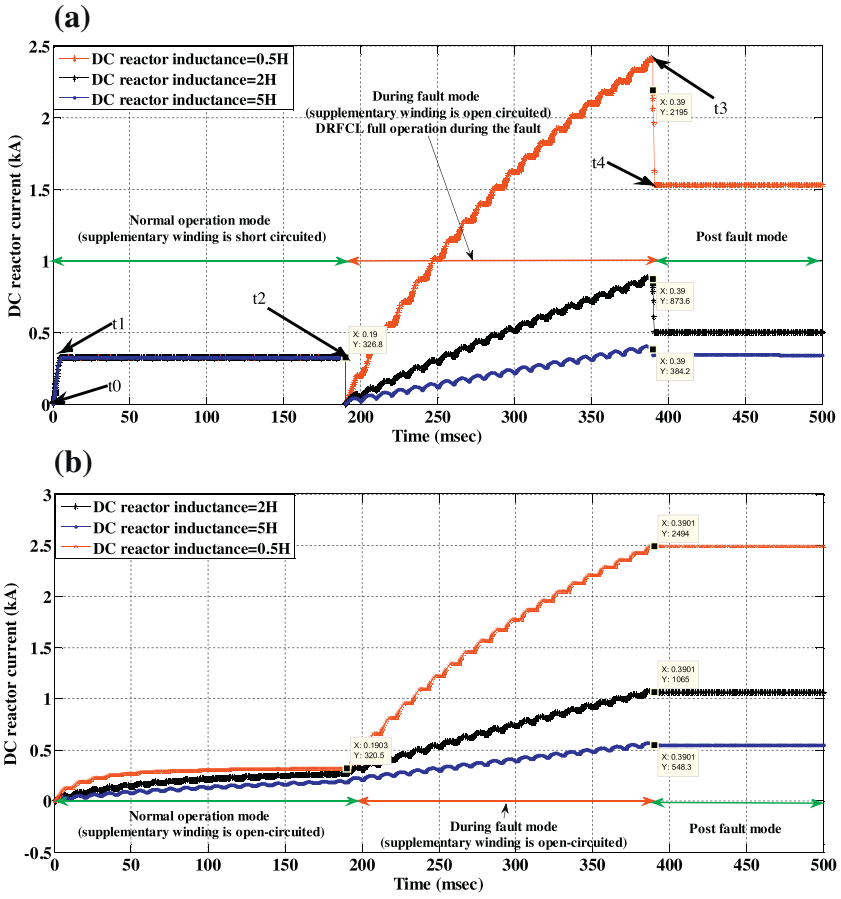

Fig. 10. DC reactor current with different DC reactor inductances (a) supplementary winding is open and (b) supplementary winding is short-circuited.

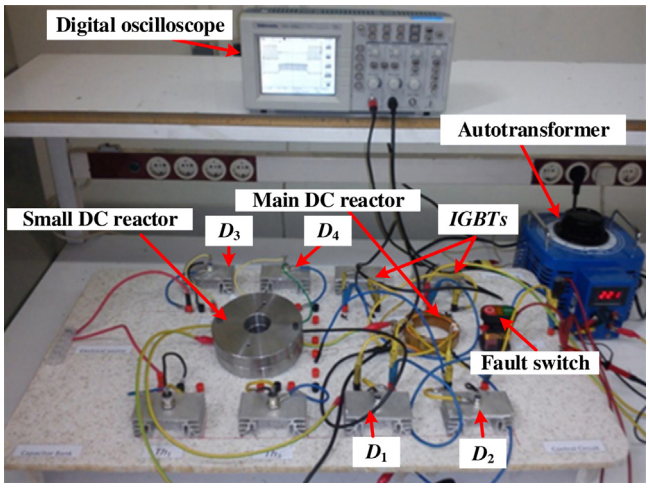

Fig. 11. DRFCL laboratory test setup.

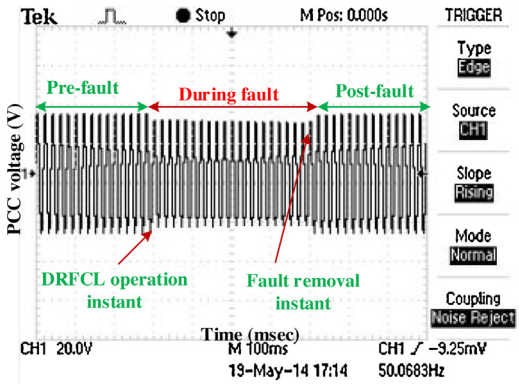

Fig. 13. PCC voltage during normal and fault operation modes (voltage/division = 20 V with probe X10 and time/division = 100 ms).

Fig. 14 shows the line current and load voltage before and after fault occurrence. The fault occurs at instant (a) shown in the figure and is removed at instant (b). Before the fault occurrence, the line current amplitude is 1 A and the load voltage is 220 V. The load voltage and line current are sinusoidal and system works under normal condition. In this case, the voltage drop on DRFCL is negligible. At the instant of the fault occurrence, the fault current is decreased to 4 A as shown in Fig. 14. After fault removal, the DRFCL voltage drop is zero and the system works under normal Condition again. Fig. 14 is in good agreement with Fig. 9.

The suggested DRFCL has a fast response by using controllable DC reactor. In Fig. 15, the effect of the supplementary winding of the DC reactor on the network steady state response is shown. Fig. 15(a) illustrates the DC reactor current rise after CB energization while the supplementary winding is open both in normal and fault operation modes. In Fig. 15(b), the DC reactor current rise after CB energization is shown while the supplementary winding is short circuited during normal operation mode and is opened during the fault.

The measured current waveform shows the considerable delay of the DC reactor charging when the supplementary winding is not short circuited. These experimental results are in agreement with the simulation results shown in Fig. 10(a) and (b). In practice, when the DC reactor freewheels in the steady state, it seems to be short circuited.

After CB energization, the proposed network works under normal condition and the DC reactor is bypassed, so its current is I_{dc} with a small ripple as shown in Fig. 16. After fault occurrence, the DC reactor current rises and the increased current in the reactor winding is brought out of saturation. The unsaturated reactor presents a considerable inductance in series with the line and the fault current is accordingly decreased. Fig. 16(a) shows the DC reactor current and load voltage before, during and after fault and Fig. 16(b) shows the DC reactor current in two repetitive fault cases. As shown in this figure, the DRFCL can successfully control the fault current in the case of repetitive fault occurrence.

The advantages of the proposed DRFCL in comparison with other DC reactor type FCLs, can be stated as follows:

- In comparison with the FCLs presented in [14–18], the proposed DRFCL uses only one DC reactor to restrain the PCC voltage and control the fault current amplitude with high inductance, which enables a simpler operation by opening and closing the supplementary winding circuit, less power losses in the steady state, very fast response to fault occurrence and consistency in fault current suppression.
- Although the DC reactor is inserted in series with the line, between the voltage source and the load, it will not cause resonance problems, since it is almost invisible during the steady state and will not affect the steady-state performance of the network.
- The configuration of the DRFCL is simple and reliable because its operation is based on the series reactor and rectifier bridge.
- There is no need for any additional control or detection circuit therefore, the response of this DRFCL is so fast and the total cost of DRFCL is considerably decreased.
- As long as the amplitude of the DC reactor current is greater than that of the line current, the proposed DRFCL keeps the original performance under unbalanced fault condition.
- The proposed DRFCL not only restrains the PCC voltage drop but also limits the fault current when a fault occurs at the load side. Furthermore, it can reduce the interrupting rating of the circuit breaker.
- By proper switching of IGBTs, the DRFCL does not need bias voltage source because these switches can quickly open circuit the main winding by opening the circuit of the supplementary winding and also rapidly force the DC reactor into short circuit state by closing the supplementary winding circuit.
- In addition, power losses and voltage drop on switches must be taken into account during the fault. The suggested topology can

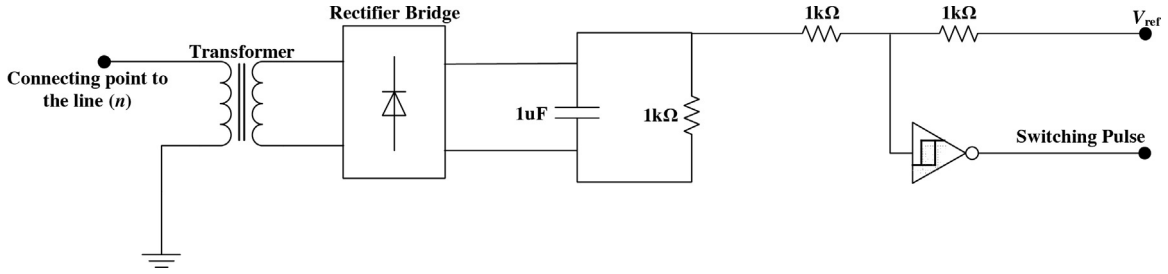

Fig. 12. IGBTs control circuit.

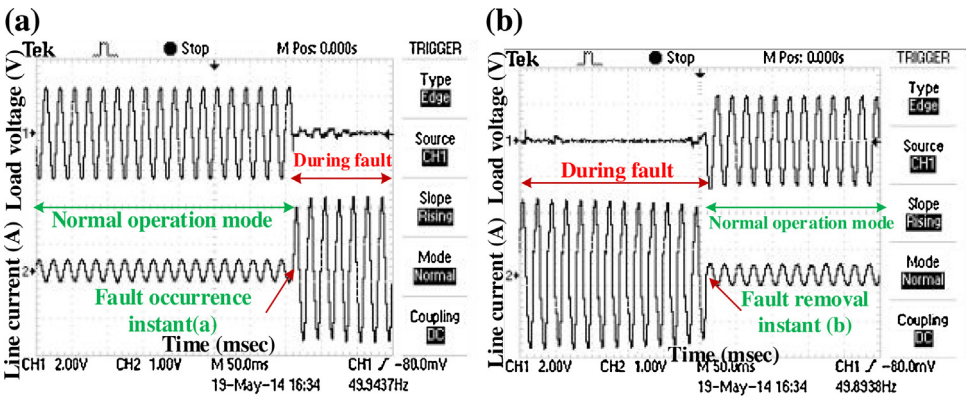

Fig. 14. DRFCL effect on line current and load voltage before and after fault occurrence (voltage/division = 2 V with probe X100 for CH1, current/division = 1 V with probe X1 for CH2 and time/division = 50 ms).

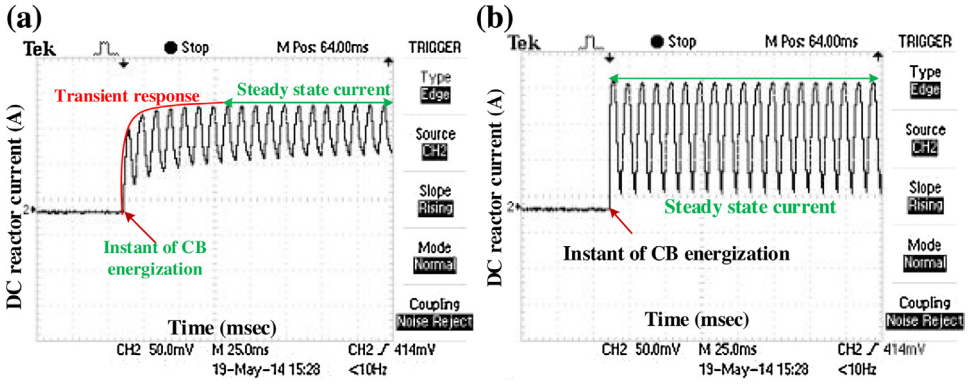

Fig. 15. DC reactor current after CB energization (a) supplementary winding of DC reactor is open circuited (b) supplementary winding is short circuited after CB energization and is open circuit in steady state and fault operation modes (current/division = 50 mA with probe X100 and time/division = 25 ms).

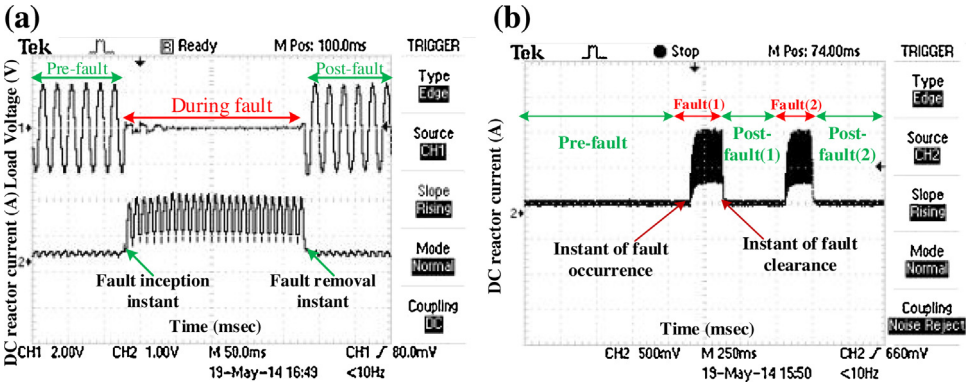

Fig. 16. (a) DC reactor current and load voltage during normal and fault operation modes (measured DC reactor current (lower curve) and load voltage (upper curve) during normal and fault operation modes while supplementary winding is short-circuited during normal operation and is open-circuited in fault operation mode). (b) DC reactor current during repetitive fault case (where (voltage/division = 2 V with probe X100 for CH1, current/division = 1 A with probe X10 for CH2 and time/division = 50 ms).

employ the self-turn off switch for switching implementation just in a short time. Also, series–parallel connections of semiconductor switches have been recently introduced to satisfy the requirements of a wide range of voltage and current levels.

6. Conclusion

This paper presented a novel DC reactor-type fault current limiter (DRFCL) to reduce the fault current and improve the PCC voltage. In the paper, the analytical study of the proposed DRFCL has been developed. Unlike other DC reactor-type FCLs, the proposed DRFCL has a simple circuit topology and there is no need for any additional control circuit. Novelty of the suggested DRFCL is the application of a high inductance DC reactor, which does not have any additional delay. This application is based on using supplementary winding with two antiparallel IGBT switches. The application of this scheme introduces a new DRFCL with fast response to the fault and fast recovery speed after fault removal. It reduces complexity and increases the system reliability. A point that should be noted is that it needs fewer components as compared with other DC reactor type FCLs and considering its simple structure, the total cost of the DRFCL is decreased. Since the DRFCL provides high impedance during the fault period, the amplitude of the fault current can be effectively decreased. During the steady-state period,

the DC reactor freewheels, the PCC voltage remains fix and there is no sever voltage drop during the fault period. The installation of the DRFCL almost will not result in voltage and current distortions, or power quality problems. According to simulation and experimental results, it has been shown that the proposed DRFCL is effective for fault current limiting and restoring the PCC voltage to the acceptable level. Furthermore, the proposed DRFCL can return the system to the normal state after fault removal as well. In addition, the advantage of this DRFCL is that neither controlled equipments nor fault detection circuits are needed since it acts automatically when the fault occurs.

Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.epsr.2015.01.005.

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